



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/872,830	05/31/2001	B. Arlen Young	ADPT1047	3668

7590 12/19/2003

Forrest Gunnison
Gunnison, McKay & Hodgson, L.L.P.
1900 Garden Road, Suite 220
Monterey, CA 93940

EXAMINER

CLEARY, THOMAS J

ART UNIT	PAPER NUMBER
----------	--------------

2111

DATE MAILED: 12/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/872,830

Applicant(s)

YOUNG, B. ARLEN

Examiner

Thomas J. Cleary

Art Unit

2181

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 May 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
- a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Figure 1 Number 122, Figure 2 Number 306, and Figure 2 Number 310. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 2, 3, 4, 5, 11, 12, 13, 14, 15, 16, 17, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 5,659,690 to Stuber et al.

("Stuber") in view of knowledge commonly known in the art, as evidenced by the Free On-Line Dictionary of Computing.

4. In reference to Claim 1, Stuber teaches a method for accessing hardware I/O control blocks, which are stored in a hardware I/O control block array, by a parallel SCSI host adapter (See Column 18 Lines 23-24). Stuber does not teach addressing one page in a plurality of pages of said hardware I/O control block array for said parallel SCSI host adapter using a first portion of a hardware I/O control block array pointer in said parallel SCSI host adapter wherein said one page includes a plurality of storage sites for hardware I/O control blocks; and addressing a hardware I/O control block stored in said one page using a second portion of said hardware I/O control block array pointer in said parallel SCSI host adapter. Stuber teaches storing the control blocks on a page. However, there are only four pages and each page can only hold one block (See Column 18 Lines 11-12 and Column 18 Lines 39-46). The availability of only four active control blocks causes I/O bottlenecks in several situations. The Examiner takes Official Notice that the use of pages in a memory system that are accessed by splitting the address into a page number, as represented by the most significant bits of the address, and an offset within that page, as represented by the least significant bits of the address, in order to allow multiple items to be stored on a page is well known in the art. This is shown to have been well known in the art at the time the invention was made by The Free On-Line Dictionary of Computing (See entry for "paging"). Further, it

is well known in the art that a pointer is an address, as evidenced by The Free On-Line Dictionary of Computing (See entry for "pointer").

One of ordinary skill in the art at the time the invention was made would construct the device of Stuber using a paging system to store the hardware I/O control blocks, resulting in the invention of Claim 1, in order to increase the available memory space by moving infrequently used I/O control blocks from the main memory to a secondary memory (See entry for "paging" of The Free On-Line Dictionary of Computing), as well as to reduce the bottlenecks that can occur by having only four active control blocks.

5. In reference to Claim 2, Stuber teaches the limitations as applied to Claim 1 above. Stuber further teaches that for tagged commands, the number of SCBs to the same target/channel/LUN may equal the space in the SCB array. The tag is then used to match the correct target/channel/LUN upon reconnection (See Column 19 Lines 44-49). Therefore, the tag is inherently used to indicate the location of the hardware I/O control block, and functions in a matter analogous to the second portion of the hardware I/O control block array pointer.

One of ordinary skill in the art at the time the invention was made would construct the device of Stuber using a paging system to store the hardware I/O control blocks, resulting in the invention of Claim 2, in order to increase the available memory space by moving infrequently used I/O control blocks from the main memory to a secondary memory (See entry for "paging" of The Free On-Line Dictionary of Computing), as well as to reduce the bottlenecks that can occur by having only four active control blocks.

6. In reference to Claim 3, Stuber teaches the limitations as applied to Claim 1 above. Stuber further teaches a reconnecting target providing a sequencer with its target and LUN addresses (See Column 119 Lines 56-60). Because the sequencer must search the entire SCB array with the target and LUN addresses until it finds a match, it must inherently store said addresses (See Column 119 Lines 56-67).

One of ordinary skill in the art at the time the invention was made would construct the device of Stuber using a paging system to store the hardware I/O control blocks, resulting in the invention of Claims 3, in order to increase the available memory space by moving infrequently used I/O control blocks from the main memory to a secondary memory (See entry for "paging" of The Free On-Line Dictionary of Computing), as well as to reduce the bottlenecks that can occur by having only four active control blocks.

7. In reference to Claim 4, Stuber teaches the limitations as applied to Claim 3 above. Stuber further teaches comparing the reconnecting target and LUN addresses stored in the sequencer with the target and LUN addresses of the SCB's in the SCB array (See Column 119 Lines 56-67).

One of ordinary skill in the art at the time the invention was made would construct the device of Stuber using a paging system to store the hardware I/O control blocks, resulting in the invention of Claim 4, in order to increase the available memory space by moving infrequently used I/O control blocks from the main memory to a secondary memory (See entry for "paging" of The Free On-Line Dictionary of Computing), as well as to reduce the bottlenecks that can occur by having only four active control blocks.

Art Unit: 2181

8. In reference to Claim 5, Stuber teaches the limitations as applied to Claim 4 above. Stuber further teaches continuing the SCB and loading the information in the SCB upon determining that the reconnecting target and LUN addresses stored in the sequencer and the target and LUN addresses of the SCB are equal (See Column 119 Lines 60-67).

One of ordinary skill in the art at the time the invention was made would construct the device of Stuber using a paging system to store the hardware I/O control blocks, resulting in the invention of Claim 5, in order to increase the available memory space by moving infrequently used I/O control blocks from the main memory to a secondary memory (See entry for "paging" of The Free On-Line Dictionary of Computing), as well as to reduce the bottlenecks that can occur by having only four active control blocks.

9. In reference to Claim 11, Stuber teaches a method for accessing hardware I/O control blocks, which are stored in a hardware I/O control block array, by a parallel SCSI host adapter (See Column 18 Lines 23-24). Stuber does not teach storing hardware I/O control blocks for targets on a SCSI bus in a paged hardware I/O control block array; and accessing one hardware I/O control block in said paged hardware I/O control block array addressed by a hardware I/O control block array pointer, wherein said hardware I/O control block array pointer includes a page identifier and a storage site identifier. Stuber teaches storing the control blocks on a page. However, there are only four pages and each page can only hold one block (See Column 18 Lines 11-12 and Column 18 Lines 39-46). The availability of only four active control blocks causes I/O bottlenecks in

several situations. The Examiner takes Official Notice that the use of pages in a memory system that are accessed by splitting the address into a page number, as represented by the most significant bits of the address, and an offset within that page, as represented by the least significant bits of the address, in order to allow multiple items to be stored on a page is well known in the art. This is shown to have been well known in the art at the time the invention was made by The Free On-Line Dictionary of Computing (See entry for "paging"). Further, it was well known in the art at the time the invention was made that a pointer is an address, as evidenced by The Free On-Line Dictionary of Computing (See entry for "pointer").

One of ordinary skill in the art at the time the invention was made would construct the device of Stuber using a paging system to store the hardware I/O control blocks, resulting in the invention of Claim 11, in order to increase the available memory space by moving infrequently used I/O control blocks from the main memory to a secondary memory (See entry for "paging" of The Free On-Line Dictionary of Computing), as well as to reduce the bottlenecks that can occur by having only four active control blocks.

10. In reference to Claim 12, Stuber teaches the limitations as applied to Claim 11 above. Stuber does not teach configuring said page identifier to identify a page in said paged hardware I/O control block array so that said paged hardware I/O control block array pointer addresses one hardware I/O control block page in said array. As described in reference to Claim 11 above, pages in a memory system are accessed by splitting the address into a page number, as represented by the most significant bits of

the address, and an offset within that page, as represented by the least significant bits of the address, in order to allow multiple items to be stored on a page is well known in the art.

One of ordinary skill in the art at the time the invention was made would construct the device of Stuber using a paging system to store the hardware I/O control blocks, resulting in the invention of Claim 12, in order to increase the available memory space by moving infrequently used I/O control blocks from the main memory to a secondary memory (See entry for "paging" of The Free On-Line Dictionary of Computing), as well as to reduce the bottlenecks that can occur by having only four active control blocks.

11. In reference to Claim 13, Stuber teaches the limitations as applied to Claim 12 above. Stuber further teaches that for tagged commands, the number of SCB's to the same target/channel/LUN may equal the space in the SCB array. The tag is then used to match the correct target/channel/LUN upon reconnection (See Column 19 Lines 44-49). Therefore, the tag is inherently used to indicate the location of the hardware I/O control block, and functions in a matter analogous to the storage site identifier of the hardware I/O control block array pointer. Stuber further teaches that the sequencer compares the tag to SCBs currently stored in the array, and thus the tag value is inherently stored (See Column 19 Lines 46-49).

One of ordinary skill in the art at the time the invention was made would construct the device of Stuber using a paging system to store the hardware I/O control blocks, resulting in the invention of Claim 13, in order to increase the available memory space

by moving infrequently used I/O control blocks from the main memory to a secondary memory (See entry for "paging" of The Free On-Line Dictionary of Computing), as well as to reduce the bottlenecks that can occur by having only four active control blocks.

12. In reference to Claim 14, Stuber teaches the limitations as applied to Claim 13 above. Stuber further teaches comparing the reconnecting target and LUN addresses stored in the sequencer with the target and LUN addresses of the SCB's in the SCB array (See Column 119 Lines 56-67).

One of ordinary skill in the art at the time the invention was made would construct the device of Stuber using a paging system to store the hardware I/O control blocks, resulting in the invention of Claim 14, in order to increase the available memory space by moving infrequently used I/O control blocks from the main memory to a secondary memory (See entry for "paging" of The Free On-Line Dictionary of Computing), as well as to reduce the bottlenecks that can occur by having only four active control blocks.

13. In reference to Claim 15, Stuber teaches the limitations as applied to Claim 14 above. Stuber further teaches retrieving the SCB upon determining that the reconnecting target and LUN addresses stored in the sequencer and the target and LUN addresses of the SCB are equal (See Column 119 Lines 60-67).

One of ordinary skill in the art at the time the invention was made would construct the device of Stuber using a paging system to store the hardware I/O control blocks, resulting in the invention of Claim 15, in order to increase the available memory space

by moving infrequently used I/O control blocks from the main memory to a secondary memory (See entry for "paging" of The Free On-Line Dictionary of Computing), as well as to reduce the bottlenecks that can occur by having only four active control blocks.

14. In reference to Claim 16, Stuber teaches a sequencer (See Figure 4 Number 320 and Column 2 Lines 53-55); and a memory including a hardware I/O control block array (See Figure 2 Numbers 240 and 243 and Column 9 Lines 17-23). Stuber does not teach a paged hardware I/O control block array pointer coupled to said sequencer and to said memory; said hardware I/O control block array being paged; and a plurality of pages going from lowest page to highest page. Stuber teaches storing the control blocks on a page. However, there are only four pages and each page can only hold one block (See Column 18 Lines 11-12 and Column 18 Lines 39-46). The availability of only four active control blocks causes I/O bottlenecks in several situations. The Examiner takes Official Notice that the use of pages in a memory system that are accessed by splitting the address into a page number, as represented by the most significant bits of the address, and an offset within that page, as represented by the least significant bits of the address, in order to allow multiple items to be stored on a page is well known in the art. This is shown to have been well known in the art at the time the invention was made by The Free On-Line Dictionary of Computing (See entry for "paging"). Further, it is well known in the art that a pointer is an address, as evidenced by The Free On-Line Dictionary of Computing (See entry for "pointer"). Stuber further teaches that the available space in the SCB array is equal to the number of unique tags that can be

returned upon reconnection of a target (See Column 19 Lines 44-49). The SCB array of Stuber is analogous to a single page of a paged system, specifically, the page currently paged-in. Therefore, Stuber teaches the number of hardware I/O block storage sites on one of the pages is equal to the number of unique tag values that can be returned by a tagged queue SCSI target reconnecting to said parallel SCSI host adapter.

One of ordinary skill in the art at the time the invention was made would construct the device of Stuber using a paging system to store the hardware I/O control blocks, resulting in the invention of Claim 16, in order to increase the available memory space by moving infrequently used I/O control blocks from the main memory to a secondary memory (See entry for "paging" of The Free On-Line Dictionary of Computing), as well as to reduce the bottlenecks that can occur by having only four active control blocks.

15. In reference to Claim 17, Stuber teaches the limitations as applied to Claim 16 above. Stuber does not teach that the memory is external to the parallel SCSI host adapter. Stuber does teach a memory that is internal to the parallel SCSI host adapter (See Figure 4 Number 340). The invention of Claim 17 would perform equally well with an internal memory, as in the prior art. Both the external memory and the internal memory accomplish the same result, viz. providing a storage means for the hardware I/O control block array. The external memory appears to offer no advantage over the prior art's internal memory and therefore it makes no difference which arrangement is used. Further, the mere fact that a structure is integral does not preclude its consisting of various elements.

One of ordinary skill in the art at the time the invention was made would construct the device of Stuber using a paging system to store the hardware I/O control blocks, resulting in the invention of Claim 17, in order to increase the available memory space by moving infrequently used I/O control blocks from the main memory to a secondary memory (See entry for "paging" of The Free On-Line Dictionary of Computing), as well as to reduce the bottlenecks that can occur by having only four active control blocks.

16. In reference to Claim 18, Stuber teaches the limitations as applied to Claim 16 above. Stuber further teaches a memory that is internal to the parallel SCSI host adapter (See Figure 4 Number 340).

One of ordinary skill in the art at the time the invention was made would construct the device of Stuber using a paging system to store the hardware I/O control blocks, resulting in the invention of Claim 18, in order to increase the available memory space by moving infrequently used I/O control blocks from the main memory to a secondary memory (See entry for "paging" of The Free On-Line Dictionary of Computing), as well as to reduce the bottlenecks that can occur by having only four active control blocks.

In reference to Claim 19, Stuber teaches an expanded SCSI control block array for a parallel SCSI host adapter (See Figure 4 Number 443); and a plurality of SCSI control block storage sites (See Column 18 Lines 11-12). Stuber does not teach a plurality of pages going from lowest page to highest page. Stuber teaches storing the control blocks on a page. However, there are only four pages and each page can only

hold one block (See Column 18 Lines 11-12 and Column 18 Lines 39-46). The availability of only four active control blocks causes I/O bottlenecks in several situations. The Examiner takes Official Notice that the use of pages in a memory system that are accessed by splitting the address into a page number, as represented by the most significant bits of the address, and an offset within that page, as represented by the least significant bits of the address, in order to allow multiple items to be stored on a page is well known in the art. This is shown to have been well known in the art at the time the invention was made by The Free On-Line Dictionary of Computing (See entry for "paging"). Stuber further teaches that the available space in the SCB array is equal to the number of unique tags that can be returned upon reconnection of a target (See Column 19 Lines 44-49). The SCB array of Stuber is analogous to a single page of a paged system, specifically, the page currently paged-in. Therefore, Stuber teaches the number of SCSI control block storage sites on one of the pages is equal to the number of unique tag values that can be returned by a tagged queue SCSI target reconnecting to said parallel SCSI host adapter.

One of ordinary skill in the art at the time the invention was made would construct the device of Stuber using a paging system to store the hardware I/O control blocks, resulting in the invention of Claim 19, in order to increase the available memory space by moving infrequently used I/O control blocks from the main memory to a secondary memory (See entry for "paging" of The Free On-Line Dictionary of Computing), as well as to reduce the bottlenecks that can occur by having only four active control blocks.

17. Claims 6, 7, 8, 9, and 10, is rejected under 35 U.S.C. 103(a) as being unpatentable over Stuber and knowledge commonly known in the art, as evidenced by the Free On-Line Dictionary of Computing, as applied to Claim 4 above, and further in view of US Patent Number 6,373,737 to Lysinger et al. ("Lysinger").

18. In reference to Claim 6, Stuber teaches the limitations as applied to Claim 4 above. Stuber does not teach changing said first portion of said hardware I/O control block array pointer upon said target address and said reconnecting target address being unequal. Lysinger teaches a content-addressable memory wherein the address currently being compared in a memory module is changed upon determination that the data at that address does not match the data being compared to it (See Column 1 Lines 66-67 and Column 2 Lines 1-4). Content-addressable memories are known in the art to be commonly used in paged-memory systems, as evidenced by The Free On-Line Dictionary of Computing (See entries for "content addressable memory" and "Memory Management Unit").

One of ordinary skill in the art at the time the invention was made would combine the device of Stuber with the content addressable memory of Lysinger, resulting in the inventions of Claim 6, in order to provide a content addressable memory for the paging system that will provide access to a relatively large number of entries at a reasonably fast rate while being simple in design and relatively inexpensive (See Column 1 Lines 58-65 of Lysinger).

19. In reference to Claims 7 and 8, Stuber and Lysinger teach the limitations as applied to Claim 6 above. Stuber does not teach addressing another page in said plurality of pages of said hardware I/O control block array for said parallel SCSI host adapter using a first portion of a hardware I/O control block array pointer in said parallel SCSI host adapter wherein said one page includes a plurality of storage sites for hardware I/O control blocks; and addressing a hardware I/O control block stored in said one page using a second portion of said hardware I/O control block array pointer in said parallel SCSI host adapter. As shown in Claim 1 above, the use of pages in a memory system that are accessed by splitting the address into a page number, as represented by the most significant bits of the address, and an offset within that page, as represented by the least significant bits of the address, is well known in the art, as evidenced by The Free On-Line Dictionary of Computing (See entry for "paging"). Further, it is well known in the art that a pointer is an address, as evidenced by The Free On-Line Dictionary of Computing (See entry for "pointer"). Stuber further does not teach that the page being addressed is another page in the plurality of pages of said hardware I/O control block array. As in Claim 6 above, Lysinger teaches that the address currently being compared in a memory module is changed upon determination that the data at that address does not match the data being compared to it (See Column 1 Lines 66-67 and Column 2 Lines 1-4). Because the address is changed, the device of Stuber will be operating on a different page.

One of ordinary skill in the art at the time the invention was made would combine the device of Stuber with the content addressable memory of Lysinger, resulting in the

inventions of Claims 7 and 8, in order to provide a content addressable memory for the paging system that will provide access to a relatively large number of entries at a reasonably fast rate while being simple in design and relatively inexpensive (See Column 1 Lines 58-65 of Lysinger).

20. In reference to Claim 9, Stuber and Lysinger teach the limitations as applied to Claim 8 above. As in Claim 4, Stuber further teaches comparing the reconnecting target and LUN addresses stored in the sequencer with the target and LUN addresses of the SCB's in the SCB array (See Column 119 Lines 56-67).

One of ordinary skill in the art at the time the invention was made would combine the device of Stuber with the content addressable memory of Lysinger, resulting in the inventions of Claim 9, in order to provide a content addressable memory for the paging system that will provide access to a relatively large number of entries at a reasonably fast rate while being simple in design and relatively inexpensive (See Column 1 Lines 58-65 of Lysinger).

21. In reference to Claim 10, Stuber and Lysinger teach the limitations as applied to Claim 9 above. As in Claim 5, Stuber further teaches retrieving the SCB upon determining that the reconnecting target and LUN addresses stored in the sequencer and the target and LUN addresses of the SCB are equal (See Column 119 Lines 60-67).

One of ordinary skill in the art at the time the invention was made would combine the device of Stuber with the device of Lysinger, resulting in the inventions of Claim 10, in order to provide a content addressable memory for the paging system that will provide access to a relatively large number of entries at a reasonably fast rate while being simple in design and relatively inexpensive (See Column 1 Lines 58-65 of Lysinger).


Conclusion


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 703-305-5824. The examiner can normally be reached on Monday-Thursday (8-5:30), Alt. Fridays (8-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-5631.

tjc


Thomas J. Cleary
Patent Examiner
Art Unit 2181


Primary Examiner
A. U. 2189